REMARKS

The claims remaining in the present application are Claims 37-52 and 71-79.

CLAIM REJECTIONS

DOUBLE PATENTING

Claims 37-53 and 71-79 are rejected under the judicially created doctrine of obviousness-type double patenting over claims 7-12 of U.S. Patent 6,513,110 (hereinafter, the '110 patent). Applicants respectfully traverse the rejection for the following reasons.

Applicants traverse the rejection on the grounds that the rejection fails to present a prima facie case of obviousness-type double patenting. The rejection does not establish that any variation between the inventions claimed in Claims 37-53 and 71-79 of the present application and Claims 7-12 of the '110 patent would have been obvious to one of ordinary skill in the art.

The rejection asserts that it would have be obvious to a person of ordinary skill in the art to recognize that the two sets of claims (i.e., Claims 37-53 and 71-79 of the present application and Claims 7-12 of the '110 patent) are similar because the negative or positive result of the check instruction of '110 patent allows determination of exceptions during re-ordering of

instructions. Applicants respectfully assert that this evidence does not constitute a prima facie case of obviousness-type double patenting.

Applicants respectfully assert that there are substantial variations between the inventions claimed in Claims 37-53 and 71-79 of the present application and Claims 7-12 of the '110 patent. Moreover, the rejection has not presented evidence that these variations would have been obvious to one of ordinary skill in the art. For example, the invention claimed in Claim 37 is directed to eliminating a memory operation from a sequence of instructions, which is a variation from the claims of the '110 patent. Because the rejection has not presented evidence that this variation would have been obvious to one of ordinary skill in the art, the rejection fails to present a prima facie case of obviousness-type double patenting.

Therefore, the inventions claimed in Claims 37-53 and 71-79 are not an obvious variation of the Claims 7-12 in the '110 patent.

35 U.S.C. §103

Claims 37-52 and 71-79 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sager et al., U.S. Patent No. 5,519,841 (hereinafter, Sager) in view of Tan et al., U.S. Patent No. 5,920,710 (hereinafter, Tan). The rejection is respectfully traversed for the following reasons.

Independent Claim 37 recites:

> A method of scheduling and executing instructions comprising:
> a) accessing a sequence of instructions comprising:
> a first memory operation that involves a first address range;
> a second memory operation that involves at least a portion of said first address range; and
> a third memory operation intervening said first and second memory operations, wherein it is not known whether said third memory operation involves an address within said first address range, wherein at least one of said first through third memory operations comprises a store operation;
> b) eliminating said second memory operation from said sequence of instructions;
> c) executing said sequence of instructions with said second memory operation eliminated; and
> d) determining, during said executing, if said third memory operation involves an address within said first address range, and if so, raising an exception and re-executing the sequence of instructions including said second memory operation.

Claim 37 recites, "determining, during said executing, if said third memory operation involves an address within said first address range, and if so, raising an exception and re-executing the sequence of instructions including said second memory operation." The rejection concedes that Sager fails to teach these limitations.

Tan fails to remedy this deficiency in Sager in that Tan fails to teach or suggest, "determining, during said executing, if said third memory operation involves an address within said first address range, and if so, raising an exception and re-executing the sequence of instructions including said second memory operation." The passages in Tan cited by the rejection do not teach or suggest these limitations. Applicants note that the claimed raising the

exception is dependent upon the determining if said third memory operation involves an address within said first address range.

Tan allows for out of order processing of instructions. Tan teaches a reorder buffer with temporary storage locations for results that change certain registers in order to allow out of order processing (Tan, at column 9, line 41 - column 10, line 8). However, Tan does not teach or suggest that an exception is raised if said third memory operation is determined to involve an address within said first address range, as claimed. To the contrary, this passage of Tan is teaching how to successfully execute re-ordered instructions.

Tan may teach handling exceptions (col. 8, line 62 - col. 9, line 18; and col. 20, lines 1-9). However, Tan does not teach that the exception is raised if said third memory operation is determined to involve an address within said first address range, as claimed. Thus, the rejection's reliance on multiple distinct portions of Tan's disclosure does not demonstrate that Tan teaches the claim limitations of determining, during said executing, if said third memory operation involves an address within said first address range, and if so, raising an exception and re-executing the sequence of instructions including said second memory operation.

For the foregoing reasons, neither Sager nor Tan teach determining, during said executing, if said third memory operation involves an address

within said first address range, and if so, raising an exception and re-executing the sequence of instructions including said second memory operation.

Applicants further assert that the combination of Sager and Tan fails to teach or suggest the limitations of Claim 37. In particular, one of ordinary skill in the art would not be motivated to combine Sager and Tan to arrive at the claim limitations.

Claim 37 recites a sequence of instructions comprising a first, a second, and a third memory operation. Claim 37 further recites that the second memory operation is eliminated from the sequence and the sequence of instructions is executed with said second memory operation eliminated.

For the sake of argument, Sager may teach accessing a sequence of instructions comprising a first memory operation that involves a first address range; a second memory operation that involves at least a portion of said first address range; and a third memory operation intervening said first and second memory operations, wherein it is not known whether said third memory operation involves an address within said first address range, and wherein at least one of said first through third memory operations comprises a store operation.

Further, Tan may teach canceling instructions subsequent to a mis-predicted branch instruction (Abstract). However, there is no suggestion in the art to modify Sager by eliminating the second memory operation from the sequence of instructions (to arrive at claim limitations recited in "a" and "b" of Claim 37). Applicants respectfully assert that the reason why Sager is discarding instructions is because a branch was mis-predicited. However, Claim 37 recites re-executing the sequence of instructions including said second memory operation if said third memory operation involves an address within said first address range. Thus, the second memory operation is not being eliminated because of a branch mis-prediction as in Sagar.

Further, if for the sake of argument the second memory operation were eliminated from the sequence of instructions in Sager because of a branch mis-prediction as taught by Tan, there would not be a reason to re-execute the sequence of instructions including said second memory operation if said third memory operation involves an address within said first address range, as claimed. That is, when an instruction is discarded because of a branch mis-prediction (as taught by Tan) that instruction would not be brought back. In contrast, Claim 37 recites, "determining, during said executing, if said third memory operation involves an address within said first address range, and if so, raising an exception and re-executing the sequence of instructions including said second memory operation."

For the foregoing reasons, the combination of Sager and Tan do not teach or suggest the limitations of Claim 37.

Applicants respectfully assert that neither Sager nor Tan, alone or in combination, teach or suggest the limitations of Claim 37.

Independent Claims 45, 49, 71 and 75 comprises similar limitations to those discussed in the response to Claim 37. For at least the reasons discussed in the response to Claim 37, Claims 45, 49, 71 and 75 are believed to be allowable.

Dependent Claims 38-44, 46-48, 50-52, 72-74, and 76-79 depend from Independent Claims 37, 45, 49, 71, and 75, which are believed to be allowable for the foregoing reasons. Therefore, dependent Claims 3838-44, 46-48, 50-52, 72-74, and 76-79 are believed to be allowable.

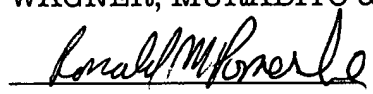
CONCLUSION

It is respectfully submitted that Claims 37-52 and 71-79 are neither taught nor suggested by the cited references and, therefore, allowance of Claims 37-52 and 71-79 is earnestly solicited.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: 3/15, 2005



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